Universidad de Alcalá

TEACHING GUIDE

Digital Electronic Systems

Degree in
Telecommunication Technologies Engineering (GITT)
Telecommunication Systems Engineering (GIST)
Telematics Engineering (GIT)
Electronic Communications Engineering (GIEC)

Universidad de Alcalá

Academic Year 2020/2021

3rd Year - 1st Semester (GITT+GIST+GIT+GIEC)

Approved by the School Board on June 24, 2020

TEACHING GUIDE

Course Name:	**Digital Electronic Systems**
Code:	**350014 (GITT+GIST+GIT+GIEC)**
Degree in:	**Telecommunication Technologies Engineering (GITT)** **Telecommunication Systems Engineering (GIST)** **Telematics Engineering (GIT)** **Electronic Communications Engineering (GIEC)**
Department and area:	**Electrónica** **Electronic Technology**
Type:	**Compulsory (GITT+GIST+GIT+GIEC)**
ECTS Credits:	**6.0**
Year and semester:	**3rd Year - 1st Semester (GITT+GIST+GIT+GIEC)**
Teachers:	See website: https://www.uah.es/es/estudios/estudios-oficiales/grados/asignatura/index.html?codAsig=350014
Tutoring schedule:	See website
Language:	English

1. COURSE SUMMARY

Digital Electronic Systems aims to introduce students to the design of digital systems that are based on a microprocessor. This module is essentially concerned with the study of microprocessors, semiconductor memories, input/output systems and their associated circuits for the construction of built-in systems. It therefore draws on the study of digital electronics with the introduction of programmable systems and data storage systems. The module covers topics related to both hardware (use of peripheral, timers, interruptions, etc.) and software (organisation of memory, addressing modes, peripheral mapping, etc.).

In order to benefit the students fully from this module, they must possess prior knowledge acquired from the Digital Electronics module, which ran in the second semester of the second year, as the basic concepts of that module also apply to Digital Electronic Systems module.

2. SKILLS

Basic, Generic and Cross Curricular Skills.

This course contributes to acquire the following generic skills, which are defined in the Section 3 of the Annex to the Orden CIN/352/2009:

en_TR2 - Knowledge of basic subjects and technologies that enables to learn new methods and technologies, as well as to provide versatility that allows adaptation to new situations.

en_TR3 - Aptitude to solve problems with initiative, decision making, creativity, and to communicate and to transmit knowledge, skills and workmanship, comprising the ethical and professional responsibility of the activity of the Technical Engineer of Telecommunication.

en_TRU1 - Capacity of analysis and synthesis.

en_TRU2 - Oral and written competencies.

en_TRU3 - Ability to manage information.

en_TRU4 - Autonomous learning skills.

en_TRU5 - Team work.

Professional Skills

This course contributes to acquire the following professional skills, which are defined in the Section 5 of the Annex to the Orden CIN/352/2009:

en_CT1 - Skills for autonomous learning of new concepts and techniques suitable for the conception, development or commissioning of telecommunication systems and services.

en_CT2 - Ability to use telecommunications and computing aplications (ofimatics, data bases, advanced calculus, project management, visualization, etc) in order to support the exploration and development of nets, services and aplications of telecomunications and electronic.

en_CT3 - Ability to use computer tools to search bibliographic resources or information relating to telecommunications and electronics.

en_CT9 - Ability to analyze and design combinational and sequential circuits, synchronous and asynchronous, and (partially) use of microprocessors and integrated circuits.

Learning Outcomes

RA1: Knowledge of the foundations and applications of digital electronics and microprocessors.

RA2: Knowledge of the basic elements of a digital electronic system based on a microprocessor.

RA3: Knowledge of data storage elements, particularly of semiconductor memories and select the most suitable ones to make applications with them.

RA4: Knowledge about how microprocessors and microcontrollers function and apply it in the design and development of digital electronic systems based on them.

RA5: Knowledge about how the different external elements function and are connected.

RA6: Capacity to design digital electronic systems.

3. CONTENTS

Sections of content	Total number of hours
Topic 0: Module introduction Presentation of the Module's Guide content. Explanation of the methodology of work, timings and assessment.	1 hours
Topic 1: Programmable digital electronic systems Introduction to the concept of built-in Systems, and their general characteristics. Design bases of digital systems and how microprocessors function as a nucleus of these. Brief revision of the history of microprocessors. Types of digital system development tools. Internal architecture of a microprocessor, programmer's model, instructions and addressing modes, elements of a microprocessor-based system, memory and input/output systems.	8 hours
Topic 2: The microprocessor: architecture and programming model. Introduction to the Cortex-M3: study of the generalities of the ARM, the ARM Cortex-M3 processor. Description of the Cortex-M3 architecture: detailed block diagram, typical connections, buses and interfaces. Study of its programming model and registers: low, high and special registers. Operating modes and data types. Description and generalities of the instruction set: data movement, unconditional jumps, and conditional jumps. Subroutines. Study of the Stack. Ports (general theory and ARM).	12 hours
Topic 3: The microprocessor: Exception system. Interrupts and exceptions (general theory). Study of the exceptions in the Cortex-M3: types, priority, vector tables. Description of the NVIC module: basic configuration, the reset and auto-reset, reset types. Software interrupts. Timers and counters (general theory). The SYSTICK timer, examples. Analysis of an interrupt: input and output sequences, nested interrupts, latency. Other features: power management module, multiprocessor communication.	15 hours

Topic 4: Memory management. Classification and structure of memories. Memory access chronograms. Description and implementation of memory expansion: size and number, examples. Memory maps: concept, functional and physical maps, base address. Design of a memory map: address decoding and selection logic; alternative procedures; examples of memory map designs. Memory management: bank switching; connection to the busses of the different memory banks. Data arrangement in a memory: Big and Little Endian models; aligned and non-aligned data. Timing of an external system connected to a uP. Input/output digital systems, digital interfaces (general theory and other peripherals in this microprocessor). Studying the memory map of a sample board. Data arrangement. EMC module. MPU module.	12 hours
Final practice	8 hours

4. TEACHING - LEARNING METHODOLOGIES. FORMATIVE ACTIVITIES.

4.1. Credits Distribution

Number of on-site hours:	58 hours (56 hours on-site +2 exams hours)
Number of hours of student work:	92
Total hours	150

4.2. Methodological strategies, teaching materials and resources

In the teaching and learning process the following training activities will be undertaken:

1. Theoretical Classes and example solving.
2. Practical Classes: laboratory and exercise solving.
3. Use of recorded and/or interactive videos with explanations of theory and practice.
4. Tutorials: individual and/or in groups.

The following additional resources, among others, will also be available for use:

- System for collecting quick answers to questionnaires using mobile devices to: control attendance, increase student participation, have immediate feedback with students, increase their attention, perform an evaluation, etc. It can be used in both theoretical and practical classes.
- Individual or group tasks: after completing a project, students can present it publically in front of the rest of their classmates in order to stimulate debate.
- Attendance at conferences, meetings, or scientific discussions that are related to the module content.

Along with the subject, both theoretical and practical activities and tasks will be proposed to the students. Different practical tasks will be undertaken at the same time as theoretical concepts are taught, so that students can experiment both individually and in groups, thus consolidating their knowledge of the concepts they have learned.

In order to complete these practical tasks, the students will have access to an area in the laboratory with certain basic equipment (oscilloscopes, power supplies, signal generators, etc), the necessary hardware system as well as a computer with the required design and simulation software.

In the course of the module, the students must make use of different bibliographic resources, so that they familiarise themselves with the type of documentation that they will use professionally in their future.

5. ASSESSMENT: procedures, evaluation and grading criteria

Preferably, students will be offered a continuous assessment model that has characteristics of formative assessment in a way that serves as feedback in the teaching-learning process.

5.1. PROCEDURES

The evaluation must be inspired by the criteria of continuous evaluation (Regulations for the Regulation of Teaching Learning Processes, NRPEA, art 3). However, in compliance with the regulations of the University of Alcalá, an alternative process of final evaluation is made available to the student in accordance with the Regulations for the Evaluation of Apprenticeships (approved by the Governing Council on March 24, 2011 and modified in the Board of Directors). Government of May 5, 2016) as indicated in Article 10, students will have a period of fifteen days from the start of the course to request in writing to the Director of the Polytechnic School their intention to take the non-continuous evaluation model adducing the reasons that they deem convenient. The evaluation of the learning process of all students who do not apply for it or are denied it will be done, by default, according to the continuous assessment model. The student has two calls to pass the subject, one ordinary and one extraordinary.

Ordinary call

The assessment in the ordinary call should be based on continuous assessment criteria, consistent with the acquisition of the skills specified in the subject.

a. Continuous assessment model: consists of passing the laboratory practices, completion and passing their deliveries, and passing the two Partial Evaluation Tests (PET1 and PET2) and the Final Test (FT). All of the above includes activities based on a quick answer system using mobile devices. The Lab practices and deliveries of the course will take place throughout the semester.
b. Final assessment model: It will consist of conducting the successful completion of a theoretical and practical final exam.

Extraordinary call

If the student chose the final assessment model, the assessment will be based on a theoretical and practical exam.

5.2. EVALUATION

EVALUATION CRITERIA

These criteria must address the extent to which learning outcomes for the student have been fulfilled.

CE1: The student shows the ability and initiative in solving practical problems related to the design of digital systems.

CE2: The student can make a complete digital system design, based on the definition of requirements and meeting specific criteria.

CE3: The student can analyze digital systems based on processors and memories and determine their characteristics.

CE4: The student has acquired knowledge of programmable digital systems, their structures, and composition as well as their design features.

CE5: The student is capable of designing projects of digital electronic systems, consisting of both software and hardware parts.

GRADING TOOLS

There are different tests and exercises to assess these assessment criteria. These are described below, along with the corresponding assessment criteria.

1. **Attendance** at 75% of the classes at least and participation in the activities proposed in the Virtual Classroom
2. **Two Partial Evaluation Tests (PET1 and PET2)** consisting of various questions and/or problems, about analysis and/or synthesis, referred to specific aspects of the syllabus. They can cover a portion of the lectures, exercises and laboratory.
3. **Final assessment test (FAT),** consisting of several questions and/or problems covering all the contents of the syllabus of the subject. The FAT includes two parts, PET1R and PET2R, whose contents correspond to the PET1 and PET2 tests, respectively. Students will maintain the highest score obtained between PET1 and PET1R, and PET2 and PET2R.
4. **Laboratory practices (LP) + Final practice, mandatory attendance.**The practices cover the knowledge acquired in the practical part of the course.
5. **Laboratory test (LT),** which will cover the knowledge acquired in the practical part of the course.

GRADING CRITERIA

A table for each assessment model is included below. Each table shows the relationship between the different instruments, assessment criteria, and the percentage of the grading assigned to each part.

Ordinary call, Continuous assessment model

Skill	Learning Outcomes	Evaluation criteria	Grading Tool	Contribution to the final mark
TR2, TR3, TRU1, CT1, CT9	RA1-RA5	CE2, CE3	PET1	35%
TR3, TRU1, CT1, CT9	RA1, RA3, RA5	CE1, CE4	PET2	35%
TRU3, TRU4, TRU5, CT2, CT3	RA1-RA6	CE1-CE5	LP	30%
TRU2, TRU3			Attendance at 75% of the classes and participation in the activities planned in the Virtual Classroom	

As a result, the module assessment criteria states that to pass the continuous assessment, students will need to prove that the theoretical, practical, and experimental competencies they have acquired are of an appropriate level. The following conditions must thus be fulfilled:

1. At least 75% of class attendance and participation in the activities planned in the Virtual Classroom. Otherwise, it will be understood that continuous assessment is not passed.
2. Completion of the assessment tests (PET1, PET2), proving the acquisition of skills covered by the course.
3. Pass 40% of the skills on average of all the tests devoted to the microprocessor topics (units 1 through 3).
4. Pass 40% of the skills in the average of all the tests devoted to memory management topics (unit 4).
5. Satisfactory performance in the assessment of competencies that are related to laboratory practices. A student is considered to have acquired a satisfactory knowledge of these competencies if all the following conditions are fulfilled: 1) they attend the laboratory, 2) complete all the practices, 3) acquire the skills in at least 75% of the practices as well as in the final practice and 4) their grade in the related tests is equal to or higher than 50% of the maximum mark.
6. The final weighted score (NN) of all continuous assessment tests equal to or greater than 5 out of 10, ie NN≥5, where:

   o NN = 0.35 * PET1 + 0.35 * PET2 + 0.30 * LAB

   (PET1, PET2, and LAB rated between 0 and 10 points)

   Note: If NN is equal to or greater than 5 points out of 10, but some of the above conditions (1 ~ 6) have not been met, the student will be scored with 4.5 points out of 10.

All students have the option to apply for FAT. Students will maintain the highest score obtained between PET1 and PET1R, and PET2, and PET2R.

A student is considered to have participated in the continuous assessment process, and therefore will be scored in the ordinary call, if he/she takes any of the continuous assessment tests. In other words, it will not be marked as "Absent Fail".

Ordinary call, Final assessment model

Skill	Learning Outcomes	Evaluation criteria	Grading Tool	Contribution to the final mark
CT1, CT9, TR2, TR3, TRU1, TRU2, TRU3, TRU4	RA1-RA6	CE1-CE5	FAT	70%
CT2, CT3, TR3, TRU2, TRU3, TRU4	RA1-RA6	CE1-CE5	LP	30%

To pass the course according to this model, the student must obtain at least 5 points out of 10 in each of the two previous tests.

Extraordinary call

In the case of the extraordinary call, the same percentages that have been established in the case of the evaluation by means of a final exam will be maintained, giving the option of making the PL or maintaining the mark obtained in the EL (continuous evaluation) or in the PEF (final evaluation), according to the student's decision. In any case, the PL will be made by those students who have not done it in the final exam option in the ordinary call.

Skill	Learning Outcomes	Evaluation criteria	Grading Tool	Contribution to the final mark
CT1, CT9, TR2, TR3, TRU1, TRU2, TRU3, TRU4	RA1-RA6	CE1-CE5	FAT	70%
CT2, CT3, TR3, TRU2, TRU3, TRU4	RA1-RA6	CE1-CE5	LP	30%

6. BIBLIOGRAPHY

6.1. Basic Bibliography

- The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors. 3rd Edition. Joseph Yiu. Paperback ISBN: 9780124080829. eBook ISBN: 9780124079182. 2013.
- Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C. Third Edition. Yifeng Zhu. ISBN-13: 978-0-9826926-6-0. E-Man Press LLC. July 2017.
- Fundamentos de sistemas digitales. 11 edición. Thomas L. Floyd. Editorial Pearson. 2016. Capítulo 11.
  UM10360. LPC176x/5x User manual. Rev. 4.1. NXP. 19 December 2016.
- Webpages related to the module's subject matter which will be selected in advance by the teaching staff.

6.2. Additional Bibliography

- Sistemas Digitales basados en microprocesador. MC68000. José Luis Lázaro y otros. Servicio de publicaciones de la Universidad de Alcalá. 2000.
- Sistemas de Procesamiento Digital. ZULOAGA IZAGUIRRE, Aitzol ; ASTARLOA CUELLAR, Armando. ISBN 978-84-92453-03-0. Editorial Delta. 2008.
- Microcontroller programming and interfacing: texas Instruments MSP430. Steven F. Barrett, Daniel J. Pack. ISBN 978-1-60845-713-7. Editorial Morgan&Claypool publishers. 2011.
- Fundamentos de sistemas digitales. 11 edición. Thomas L. Floyd. Editorial Pearson. 2016.

Disclosure Note

The University of Alcalá guarantees to its students that, if due to health requirements the competent authorities do not allow the total or partial attendance of the teaching activities, the teaching plans will achieve their objectives through a teaching-learning and evaluation methodology in online format, which will return to the face-to-face mode as soon as these impediments cease.